Maeesha Binte Hashem

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Education

- **University of Minnesota Twin Cities** — Minneapolis, MN
  PhD in Electrical and Computer Engineering — *Aug. 2025 - 2029. Exp*
- **University of Illinois Chicago (UIC)** — Chicago, IL
  MSc in Electrical and Computer Engineering — *Aug. 2021 - May. 2025*
- **Bangladesh University of Engineering and Technology (BUET)** — Dhaka, Bangladesh
  Bachelor of Science(B.Sc) in Electrical and Electronic Engineering — *Feb. 2015 - Apr. 2019*

Skills

- **Programming Languages**: Python, C/C++, Verilog, SystemVerilog, MATLAB.
- **Parallel Programming Languages**: Pthread, OpenMP, MPI, CUDA.
- **Scripting Languages**: TCL, Perl, Bash, Shell.
- **Machine Learning**: Deep neural network, Machine Learning, PyTorch, Tensorflow.
- **EDA Design Tool**: Cadence Genus, Innovus, Virtuoso Layout, Virtuoso Schematic, Spectre, HSPICE.
- **Simulation software**: MATLAB & Simulink, Arduino, Proteus, PSIM, PSpice, Intel Quartus Prime.

Experiences

- **Intel Corporation** — Santa Clara,CA
  System Architect and Design Engineer Intern (Co-Op) — *Jul. 2024 - Dec.2024*
  - **Project**: Designed a hardware cost model framework to evaluate and explore design space for fully digital compute in memory macros.
- **University of Illinois Chicago** — Chicago,IL
  *Graduation Research Assistant, **AEON LAB.*** — *Aug. 2021 - Jul. 2024*
  - **Memristor-based floating Point Learn-In-memory Architecture for Deep Neural Network**: Designed an energy-efficient memristor-based framework for learn-in-memory Training and inference in floating point precision.
  - **ADC/DAC-Free Analog Acceleration of Deep Neural Networks with Frequency Transformation**: Contributed to designing a low-power and computationally efficient Analog framework for DNN Inference without ADC/DAC with frequency domain model compression.
  - **Memorization-based Inference of Deep Learning**: Contributed to designing an interface for the Recurrent attention model, allowing for complex predictions to be made within a constant time and memory budget.
- **University of Illinois Chicago** — Chicago,IL
  Graduate Teaching Assistant — *Aug. 2021 - May. 2025*
  - conduct lab sessions, proctor exams, grade exam papers and projects, and hold office hours for the following courses: Introduction to VLSI Design (ECE- 467), Introduction to Embedded Systems (ECE-266), Digital Signal Processing (ECE-317), Computer Organization (ECE-366), Introduction to Logic Design (ECE-265).
- **Fermi National Accelerator Laboratory** — Chicago, IL
  Visiting MSc Student — *Jan. 2022 - May. 2022*
  - Designed a small ASIC layout in Cadence Virtuoso in 90nm; performed DRC and LVS checks.
- **Neural Semiconductor Limited & Mythic AI** — Dhaka, Bangladesh
  Associate PnR Engineer & Contractor Engineer — *Oct. 2020 - Jun. 2021*
  - Handled full-chip physical design (netlist to GDSII) of a 40nm AI chip with 500k instances, including floor planning, placement, clock tree synthesis, routing, timing, ECOs, and sign-off (DRC, LVS, LEC, ERC).
  - Developed TCL scripts for automated pin and IP block placement; modified YAML for design automation.

- **Neural Semiconductor Limited** Dhaka, Bangladesh
  Associate PnR Engineer-Trainee *Feb. 2020 - Sep. 2020*
  - Trained in fabless semiconductor manufacturing processes.
  - Performed RTL synthesis and physical Implementation (RTL to GDSII) on 45nm blocks, optimizing for frequency and power (in-house projects).
  - Automated flows and data parsing; created custom LEF, DEF, and Lib files using Bash, TCL, and Python.
  - Completed Cadence courses on Genus Synthesis Solution and Innovus Implementation System.

Publications

- Maeesha Binte Hashem, Benjamin Parpilon, Divake Kumar, Dinithi Jayasuria, and Amit Ranjan Trivedi,**"TimeFloats: Train-in-Memory with Time-Domain Floating-Point Scalar Products."** 2025 38th International Conference VLSI Design (VLSID), Kolkata, India, **2025**.
- Nethmi Jayasinghe, Maeesha Binte Hashem, Dinithi Jayasuriya, Leila Rahimifard, Min-A Kang, Vinod K. Sangwan, Mark C. Hersam and Amit Ranjan Trivedi **"Single-Step Extraction of Transformer Attention with Dual-Gated Memtransistor Crossbars"** IEEE Electron Device Letters (EDL), **2024.**
- Nastaran Darabi, Maeesha Binte Hashem, Hongyi Pan, Ahmet Cetin, Wilfred Gomes, and Amit Ranjan Trivedi, **"ADC/DAC free analog acceleration of deep neural networks with frequency transformation."** IEEE Transactions on VLSI Systems (TVLSI), **2024.**
- Davide Giacomini, Maeesha Binte Hashem, Jeremiah Suarez, Swarup Bhunia and Amit Ranjan Trivedi **"Towards Model-Size Agnostic, Compute-Free, Memorization-based Inference of Deep Learning."** 2024 37th International Conference VLSI Design (VLSID), Kolkata, India, **2024**.
- Shamma Nasrin, Maeesha Binte Hashem, Nastaran Darabi, Benjamin Parpillon, Farah Fahim, Wilfred Gomes, Amit Ranjan Trivedi,**"Memory-immersed collaborative digitization for area-efficient compute-in-memory deep learning"**, 2023 IEEE 5th International Conference on Artificial Intelligence Circuits and Systems (AICAS), Hangzhou, China, **2023**.
- Amit Ranjan Trivedi, Nastaran Darabi, Maeesha Binte Hashem and Supriyo Bandyopadhyay Trivedi,**"Exploiting Programmable Dipole Interaction in Straintronic Nanomagnet Chains for Ising Problems"**, 2023 24th International Symposium on Quality Electronic Design (ISQED), San Francisco, CA, USA, **2023**.
- Maeesha Binte Hashem, Nastaran Darabi, Supriyo Bandyopadhyay, and Amit Ranjan Trivedi,**"Solving Boolean Satisfiability with Stochastic Nanomagnets"**, 2020 29th International Conference on Electronics Circuit and Systems (ICECS), Glasgow, UK, **2022**.
- Mahmudul Hasan, Sudipto Baul, Maeesha Binte Hashem, Hamidur Rahman, **"Hardware Trojan Detection Using Slope of Path Delay Trend: Combination of Clock and DC Sweep"**, 2020 11th International Conference on Electrical and Computer Engineering (ICECE), Dhaka, Bangladesh, **2020**.
- Abir Akib, Faiza Tasnim, Disha Biswas, Maeesha Binte Hashem, Kristi Rahman, Arnab Bhattacharjee, Sheikh Anowarul Fattah,**"Unmanned Floating Waste Collecting Robot"**, 2019 IEEE Region 10 International Conference (TENCON), Kochi, India, **2019**.

Relevant Coursework

VLSI (ASIC) Design, Digital Electronics, Digital Logic Design, Computer Architecture, Advanced microprocessor Architecture and Design, High-Performance Processor & systems, Computer Algorithm, Microprocessor & interfacing, Analog Integrated Circuit, Machine Learning, Neural Network, Digital System Design, Solid State Device.